REMARKS

Applicant respectfully requests re-consideration of the application in view of the arguments presented below.

Summary of Office Action

Claims 1-16 are pending.

Claims 1-2 and 6 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,023,754 of DuLac, et al. ("DuLac") in view of U.S. Patent Application Publication No. 2004/0150581 of Westerinen, et al. ("Westerinen").

Claims 3 and 5 were rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of Westerinen and further in view of U.S. Patent No. 6,102,710 of Beilin, et al. ("Beilin").

Claim 4 was rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of Westerinen in further view of U.S. Patent Application Publication No. 2004/0059970 of Wieberdink, et al ("Wieberdink").

Claims 7-12 were rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of Westerinen in further view of U.S. Patent No. 6,752,665 of Kha, et al. ("Kha").

Claims 13 and 15 were rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of Westerinen, Kha, and Beilin.

Claim 14 was rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of Westerinen, Kha, and Wieberdink.

Claim 16 was rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of Westerinen, Kha, and U.S. Patent Application Publication No. 2003/0021232 of Duplaix, et al. ("Duplaix").

Response to 35 U.S.C. § 103 rejections

Independent claim 1 was rejected under 35 U.S.C. as being unpatentable over Dulac in view of Westerinen. Independent claim 7 was rejected under 35 U.S.C. § 103 as being unpatentable over DuLac in view of Westerinen and Kha.

With respect to an obviousness rejection under 35 U.S.C. § 103, three criteria must be met:

> *First*, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *Second*, there must be a reasonable expectation of success. *Finally*, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure

(*In re Vaeck*, 20 USPQ2d 1438; 947 F.2d 488 (Fed. Cir. 1991)(*emphasis added*)

Without regard to the first two points, applicant submits that the prior art references do not teach or suggest the claimed combination. None of the references, alone or combined, teaches or suggests *(1) controller circuit boards, (2) a storage array circuit board, and (3) a signal routing circuit board having connectors to couple the storage array circuit board and the input/output controller board.*

DuLac includes a disclosure of a bus switch for bus mapping between a host and a disk array. The bus switch selectively couples a plurality of controller busses to a plurality of drive busses. (DuLac, col. 3, lines 25-54)

Even if we assumed *arguendo* that DuLac included a disclosure of the various *circuits* (I/O controller circuit, storage array circuit, and signal routing circuit) alleged by the Examiner, there is no teaching or suggestion within DuLac as to the distribution of those circuits *across different boards*. At best, Figure 2 of DuLac illustrates a plurality of modules and electrical paths between those modules. There is no teaching or suggestion of whether the modules are distributed across more than one circuit board nor of any connectors for connecting the modules or boards in such a case.

Thus applicant respectfully submits *DuLac does not teach or suggest (1) input/output controller boards, (2) storage array circuit board, and (3) a signal routing circuit board having connectors to couple to the storage array circuit board and the input/output controller board.*

Westerinen includes a disclosure of a display monitor having multiple displays within the same housing. The monitor includes a display controller

that divides a single frame of information provided from a computer display adapter into display information for multiple displays. The display controller permits the multiple display monitor to have more panels or displays than the number of cables linking the monitor to the computer (Westerinen, par. 6).

The Examiner has stated:

> The DuLac reference fails to teach the controller circuit, storage array circuit and a signal circuit as being in different boards. As for this limitation, Westerinen et al. teaches a display controller 206 and its associated panel controller or controllers 204 as distributed over a number of different components (boards). *The reference also teaches "the functions of two or more of the components may be spread over multiple elements on the same circuit board, multiple circuit boards, or may otherwise be provided* (see paragraph 45 and Fig. 2)

(01/24/2006 Office Action, p. 3)(*emphasis added*)

The purported motivation for the combination was stated as follows:

> ...one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain an apparatus individually connecting a controller to a signal interface (via a connector) for signal conversion, as taught by Westerinen et al., (see paragraph 46)

(01/24/2006 Office Action, p. 4)(*emphasis added*)

Applicant agrees that DuLac did not teach or disclose *(1) input/output controller boards, (2) storage array circuit board, and (3) a signal routing circuit board having connectors to couple to the storage array circuit board and the input/output controller board.* The Examiner must rely on Westerinen for such elements.

Applicant notes that the "components" described by Westerinen and cited by the Examiner are neither the same as nor analogous to the claimed input/output controller board, storage array circuitry board, or a signal routing circuit board connecting the input/output controller board to the storage array circuitry board. Indeed Westerinen's monitor is an *output only* device and not a storage array.

Westerinen (paragraph 46) does not support the Examiner's motivation. Westerinen is drawn specifically to modifications required to support multiple display panels while DuLac is drawn to a controller for an

array of disk drives. Westerinen discloses use of the monitor in conjunction with a computer including disk drives (Westerinen, Fig. 2) but does not teach or suggest modifying connectivity to the computer disk drives nor introducing new functionality nor redistributing functionality to the disclosed disk storage array as has been disclosed with respect to the monitor.

Applicant respectfully submits that the stated motivation for the combination of DuLac and Westerinen is suspect at best. Westerinen appears to have been submitted solely for the general mechanical proposition that functions can be distributed across more than one physical circuit board. Applicant respectfully submits that this proposition still fails to teach or suggest the component functionality or the connectivity claimed by applicant.

Applicant thus submits the motivation for claimed combination is lacking. Even assuming *arguendo* that motivation was proper, none of the references alone or combined teaches or suggests *(1) input/output controller boards, (2) storage array circuit board, and (3) a signal routing circuit board having connectors to couple to the storage array circuit board and the input/output controller board.*

In contrast, claim 1 includes the language:

> 1. An apparatus comprising:
> *input/output (I/O) controller circuit boards;*
> *a storage array circuit board* having storage device connectors to couple storage devices to the storage array circuit board; and
> *a signal routing circuit board having one or more connectors to couple the storage array circuit board to the signal routing circuit board, connectors to couple I/O controller circuit boards to the signal routing circuit board,* and one or more multiplexers to route data signals in a selective manner along one or more first data signal paths between a first I/O controller circuit board and the storage array circuit board and along one or more second data signal paths between a second I/O controller circuit board and the storage array circuit board, wherein the second data signal path(s) share a portion of one or more data signal paths of the first data signal path(s).

(Claim 1)(*emphasis added*)

With respect to claims 7-16, applicant submits that the arguments presented above similarly apply. Although Kha was cited as an additional reference, Kha was cited only for the general proposition of introducing a

housing with removable electronic elements (01/24/2006 Office Action, pgs. 6-7).

Thus although applicant disagrees with the Examiner's characterization of Kha, even if one accepted *arguendo* the Examiner's arguments, Kha still fails to cure the deficiencies of DuLac and Westerinen. Thus none of the cited references, alone or in combination, teaches or suggests: *(1) an input/output controller board, (2) storage array circuit board, and (3) a signal routing circuit board removably connectable to the storage array circuit board and the input/output controller board.*

In contrast, claim 7 includes the language:

> 7. A storage system comprising:
> a housing;
> *a storage array circuit board* for mounting in the housing, the storage array circuit board having a plurality of storage device connectors for removably coupling a plurality of storage devices to the storage array circuit board;
> *at least one input/output (I/O) controller circuit board* for insertion in the housing, each I/O controller circuit board for communicating with storage devices; and
> *a signal routing circuit board* having electronics common to circuit boards connected thereto, *the signal routing circuit board for removable connection to the storage array circuit board and with each I/O controller circuit board,*
> wherein the electronics are removable from the housing without removal of the storage array circuit board.

(Claim 7)(*emphasis added*)

Thus claims 1 and 7 are patentable under 35 U.S.C. § 103 in view of the cited references. Given that claims 2-6 depend from claim 1 and claims 8-16 depend from claim 7, applicant submits claims 2-6 and 8-16 are likewise patentable under 35 U.S.C. § 103 in view of the cited references.

Applicant submits that the 35 U.S.C. § 103 rejections have been overcome.

Conclusion

In view of the amendments and arguments presented above, applicant respectfully submits the applicable rejections and objections have been overcome. Accordingly, claims 1-16 should be found to be in condition for allowance.

If there are any issues that can be resolved by telephone conference, the Examiner is respectfully requested to contact the undersigned at **(512) 858-9910.**

Respectfully submitted,

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